AMENDMENTS TO THE SPECIFICATION

Please replace the abstract with the following amended abstract:

An amplitude limiting circuit for limiting the amplitude of a signal input to a power amplifier includes an amplitude converter, determination unit, peak detector, window filter, delay circuit, and multiplier. The amplitude converter calculates the amplitude value of an input signal. The determination unit ~~detects, as a detection interval,~~detects an interval in which the amplitude value of the input signal exceeds ~~a threshold, on the basis of~~ a preset threshold.~~threshold and the amplitude value of the input signal.~~ The peak detector ~~detects, in the detection interval,~~detects the peak time and amplitude when the maximum amplitude appears.~~value appears and an amplitude value at the peak time as a peak value.~~ The window filter ~~generates a window function for limiting~~limits the amplitude value to ~~a value~~ not more than the threshold by using the peak value output from the peak detector. The delay circuit delays the input signal such that the peak time output from the peak detector coincides with the time when the ~~window function~~ output from the window filter exhibits the minimum value. The multiplier multiplies an output signal from the delay circuit by ~~the~~a window function. ~~An~~A CDMA communication apparatus is also disclosed.

Edited abstract, with changes:

An amplitude limiting circuit for limiting the amplitude of a signal input to a power amplifier includes an amplitude converter, determination unit, peak detector, window filter, delay circuit, and multiplier. The amplitude converter calculates the amplitude value of an input signal. The determination unit detects an interval in which the amplitude value of the input signal exceeds a preset threshold. The peak detector detects the peak time and amplitude when the maximum amplitude appears. The window filter limits the amplitude value to not more than the threshold by using the peak value output from the peak detector. The delay circuit delays the input signal such that the peak time output from the peak detector coincides with the time when the output from the window filter exhibits the minimum value. The multiplier multiplies an output signal from the delay circuit by a window function. A CDMA communication apparatus is also disclosed.